eMMC 5.1

NPE1A091-xxxG

Datasheet

Vesion:A/01

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Revision History

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1. Introduction

1.1 General Description

MM100 is an embedded MMC solution designed in a BGA package form. MM100 is a write and read device depend on MMC protocol v5.1 which is an industry standard. MM100 is easy to integration with any microprocessor with MMC host. Any kind of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This is easy to apply to market, and also MM100 series have flash rapid boot-up, high reliability, robustness, consistent performance. This series employ an industry standard eMMC 5.1 interface featuring Command Queue, HS400 interface, FFU, as well as legacy eMMC 4.51 features such as power off notifications, packed commands, Cache, boot/RPMB partitions, HPI, and HW reset, making it an optimal device for both reliable code and data storage.

1.2 Product List

Part Number	Capacity	User Area	LBA Count (Dex)	Package Size
NPE1A091-064G	64GB	62,545,461,248 Bytes	122,159,104	11.5x13x1.2mm
NPE1A091-128G	128GB	125,090,922,496 Bytes	244,318,208	11.5x13x1.2mm
NPE1A091-256G	256GB	250,181,844,992 Bytes	488,636,416	11.5x13x1.2mm

1.3 Part Number

Figure 2 MasonSemi Part Number Information

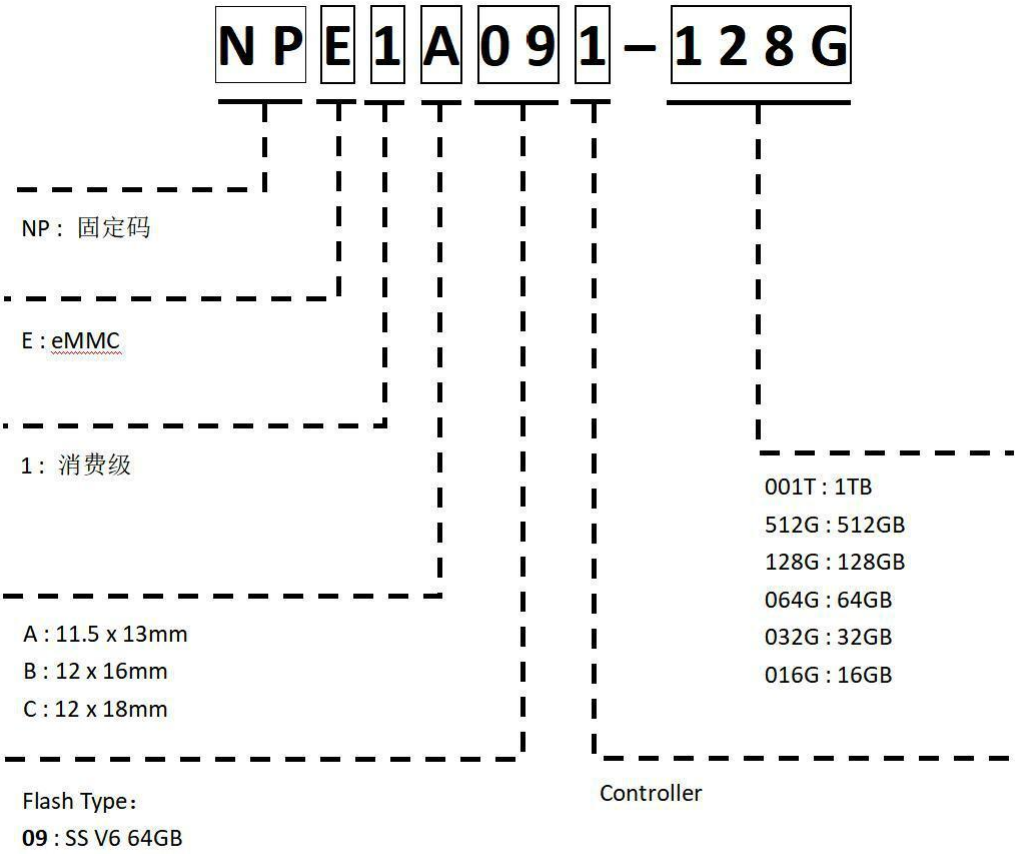
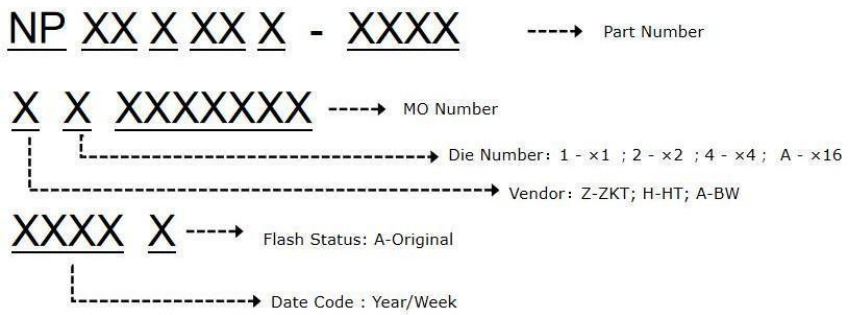


Figure 3 MasonSemi Mark Information



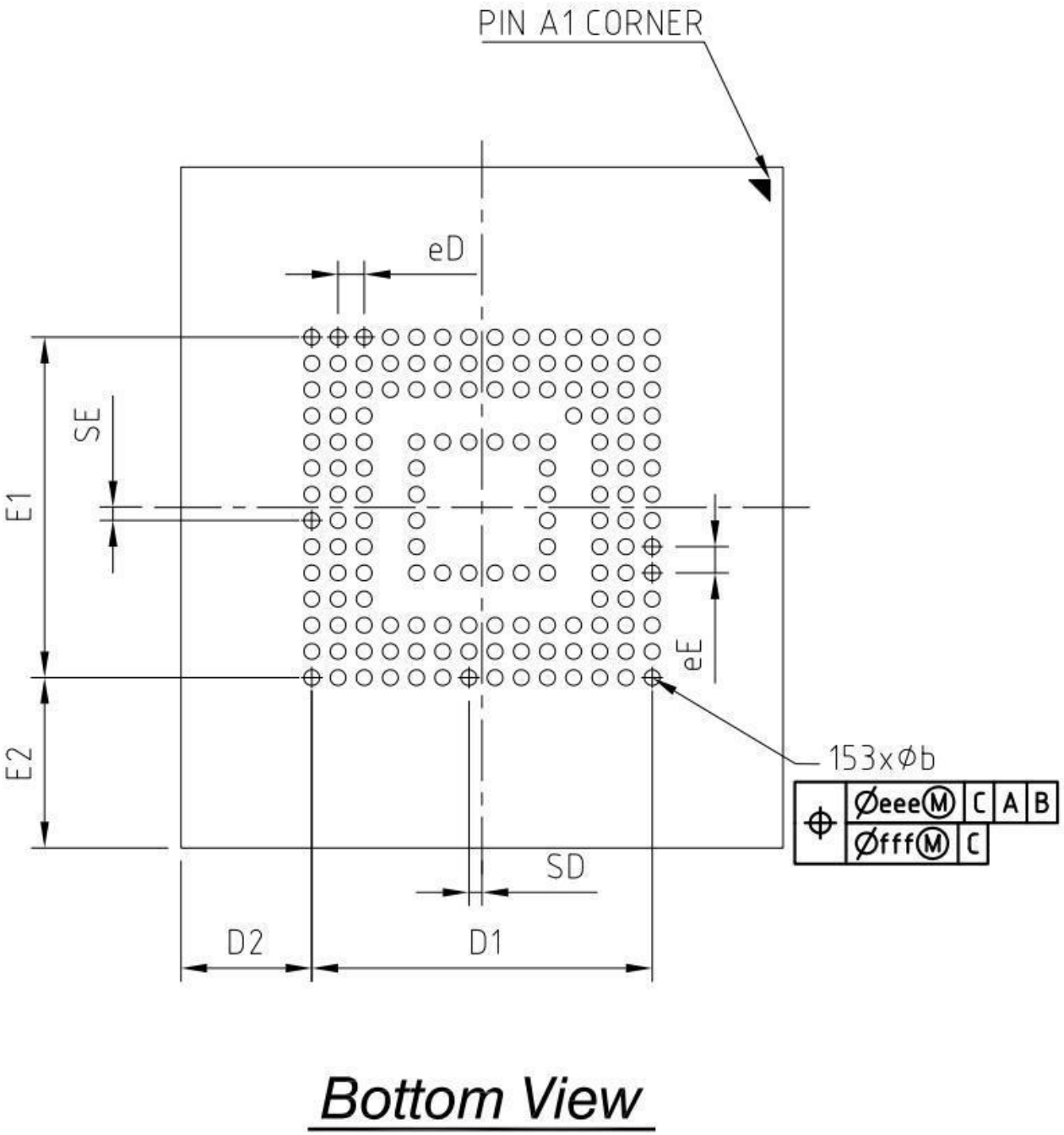
2. Key Features

- Supports eMMC 5.1
- Supports HS400 Mode
- Programmable bus width：1/4/8 bits
- Supports Boot operation in High Speed and DDR mode
- Supports Boot mode and Alternative Boot mode
- Replay Protection Memory Block (RPMB)
- Enhanced Reliable Write
- Operation Temperature：-25℃~85℃
- Storage Temperature：-40℃~85℃
- Supports a wide range of power supply voltage：1.70V~1.95V/ 2.7V~3.6V
- High Priority Interrupt (HPI)
- Secure removal types
- LDPC ECC Engine
- RoHS compliant

3. Package Configurations

3.1 BGA 153 Balls Pin Configures

Figure 1 BGA 153 Ball



3.2 Pins and Signal Description

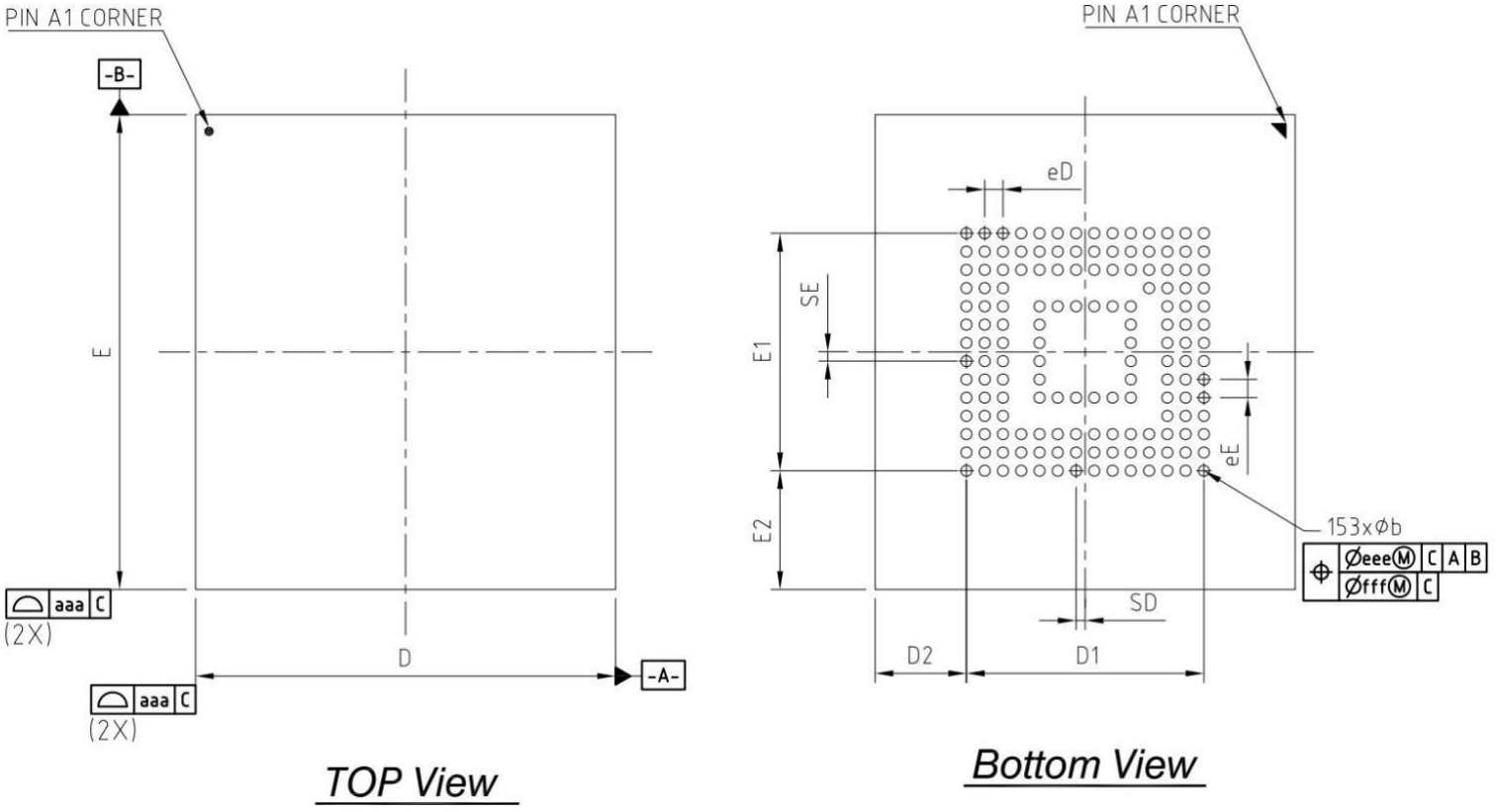
Table 1 eMMC functional pins assignment

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	VSS	N4	VCCQ
A4	DAT1	C4	VSSQ	J10	VCC	N5	VSSQ
A5	DAT2	C6	VCCQ	K5	RSTN	P3	VCCQ
A6	VSS	E6	VCC	K8	VSS	P4	VSSQ
B2	DAT3	E7	VSS	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	VSSQ
B4	DAT5	G5	VSS	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	VSS	N2	VSSQ		

- CLK: Clock input
- DS: Data Strobe is generated from eMMC to host.
- In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD: A bidirectional signal used for device initialization and command transfers.
- Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7: Bidirectional data channels. It operates in push-pull mode.
- RSTN: H/W reset signal pin
- VCC: Supply voltage for flash memory
- VCCQ: Supply voltage for memory controller
- VDDi: Internal power node to stabilize regulator output to controller core logics
- VSS: Ground connections
- NC: No Connection and left floating.

3.3 BGA Package Dimension

Figure 2 BGA 153 Balls Dimension



4. S/W Algorithm

4.1 Partition Management

MM100 initially contains two Boot Partitions and RPMB and User Data Area. The User Data Area can be divided up to four General Purpose Area to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group.

4.2 Enhanced Partition (Area)

MM100 can configure User Data Area to SLC Mode, this will enhanced user data, but the area occupies triple size of original set up size.

Max Enhanced User Data Area size can be calculate as the formula (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes).

4.3 User Density

Figure 3 Space Allocation

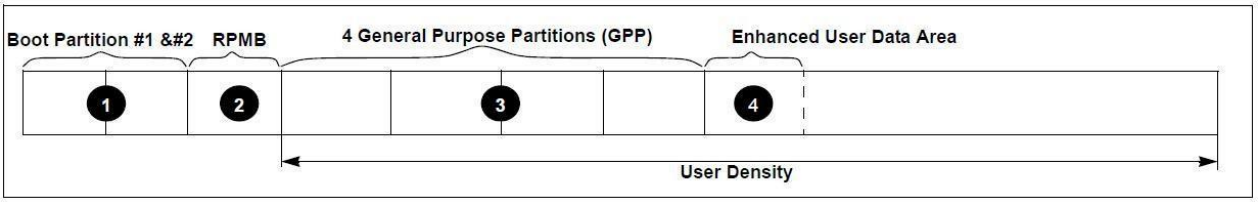


Table 2 Capacity According to Partition

	Boot partition 1	Boot partition 2	RPMB
Default.	4096KB	4096KB	4096KB
Max.	4096KB	4096KB	4096KB

4.4 Typical Performance

Table 3 Typical Performance

	Mode	64GB	128GB	256GB	Unit
Sequential Read	HS400	Up to 310	Up to 310	Up to 310	MB/s
Sequential Write		Up to 210	Up to 260	Up to 260	MB/s

Attention:

1). Performance is test with card reader, uBoot without OS.
2). Any change in testing environment may cause big difference in performance result.

5. eMMC Feature Overview

Table 4 eMMC Feature Overview

eMMC	Device Features	Function	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max Speed	Up to 400MB/s
4.41	SECURE ERASE/TRIM	“True Wipe”	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	YES
4.41	PARTITION & PROTECTION	Flexibility	YES
4.41	BACKGROUND OPERATIONS	Better user experience (low latency)	YES
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	YES
4.41	HARDWARE RESET	Robust system design	YES
4.41	HPI	Control long Reads/Writes	YES
4.41	RPMB	Secure folders	YES
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	YES
4.5	LARGE SECTOR SIZE	Potential performance	NO
4.5	PACKED COMMANDS	Reduce host overhead	YES
4.5	DISCARD	Improved performance on full media	YES
4.5	DATA TAG	Performance and/or Reliability	YES
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	YES
4.5	CACHE	Better sequential & random writes	YES
4.51	SANITIZE	“True Wipe”	YES
5.0	FIELD FIRMWARE UPGRADE (FFU)	Enables feature enhancements	YES
5.0	PRODUCTION STATE AWARENESS	Different operation during production	YES
5.0	DEVICE HEALTH	Vital NAND info	YES
5.1	ENHANCE STROBE	Sync Device and Host in HS400	YES
5.1	COMMAND QUEUE	Responsiveness	YES
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	YES
5.1	CACHE FLUSH AND BARRIER	Order cache flushing	YES
5.1	BKOPS CONTROLLER	Host control on BLOPs	YES
5.1	SECURE WP	Secure write protect	YES
5.1	EUDA	Enhance User Data Area	YES

5.1 Enhanced Reliable Write

eMMC 5.1 spec defined enhanced reliable write. Enhanced reliable write is a special write mode that old data will not be erase until new data written to the same logical address has been successfully programmed. This can ensure that the target logic address update by reliable write and never contains undefined data. When writing in enhance mode, data will remain valid even a surprise power loss happens during programming.

5.2 HS400 Mode

The 400MB/s bus speed via a 200MHz dual data rate clock frequency depends on eMMC supports HS400. HS400 mode supports 8 bits bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data.

5.3 Field Firmware Upgrade (FFU)

The field enables features enhancement by Field Firmware Updates (FFU). The host uses this mechanism to download a new firmware to the eMMC device and instructs the eMMC device to run the new downloaded firmware. The entire FFU process can work in the background without affecting the user/OS data. During the FFU process, the host can replace firmware files or single/all file systems.

5.4 Cache

The eMMC has a size of 512KB cache. This enables to improve eMMC performance for both sequential and random access.

5.5 Power off Notification

eMMC 5.1 spec defines power off notifications. The power off notifications is designed to allow the device to prepare itself to power off, and improve experience during power-on. While power off notification is enabled note that the device may be set into sleep mode.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

5.6 High Priority Interrupt(HPI)

When user launch a process, the operating system usually uses demand-paging. While in a middle of a write operation, host needs to fetch pages, the request will be delayed until the completion of the write command.

eMMC 5.1 spec defines the high priority interrupt (HPI) enables low read latency operation by suspending

a lower priority operation before it is actually completed.

5.7 Secure Erase

eMMC supports the optional Secure Erase command for backward compatibility reasons.Host can erase the provided range of LBAs and ensure no older copies of this data exist in the flash by using this command.

5.8 Secure Trim

eMMC supports Secure Trim command for backward compatibility reasons. Secure Erase supports the same function as Secure Trim, but Secure Erase has the big range than the Secure Trim.

5.9 Discard

eMMC 5.1 spec defines discard command. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of eMMC and reduce amount of housekeeping operation.

5.10 Packed Commands

eMMC 5.1 spec defines packed commands to enable optimal system performance. This allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Also, it allows reducing overall bus overheads.

5.11 Sleep

By using the SLEEP/AWAKE (CMD5), eMMC may be switched between a Sleep and a Standby state. The power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5) in the Sleep state. The memory device ignores all the other commands. The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

5.12 Sanitize

In order to remove data from the device needs Sanitize operation. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue

the sanitize operation, with busy asserted, until one of the following events occurs:

- HPI is used to abort the operation
- Sanitize operation is complete
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

6. Electrical Characteristics

6.1 Supply Voltage

Table 5 Supply Voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ(Low)	1.7	1.95	V
	VCCQ(High)	2.7	3.6	
	VCC	2.7	3.6	
	VSS，VSSQ	-0.3	0.3	

6.2 Bus Signal Levels

Figure 4 Bus Signal Levels

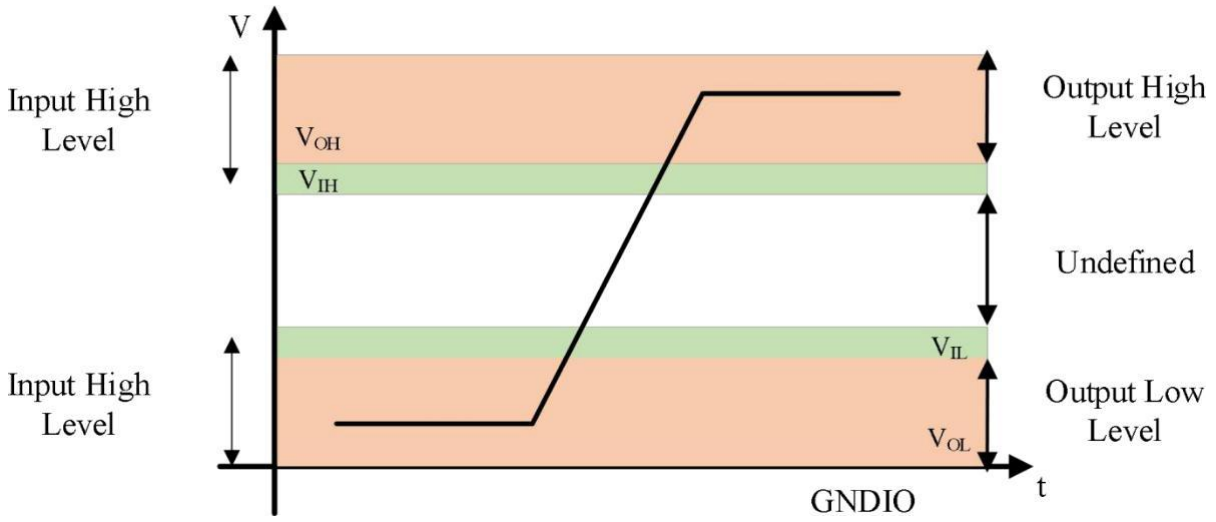


Table 6 Bus Signal Levels

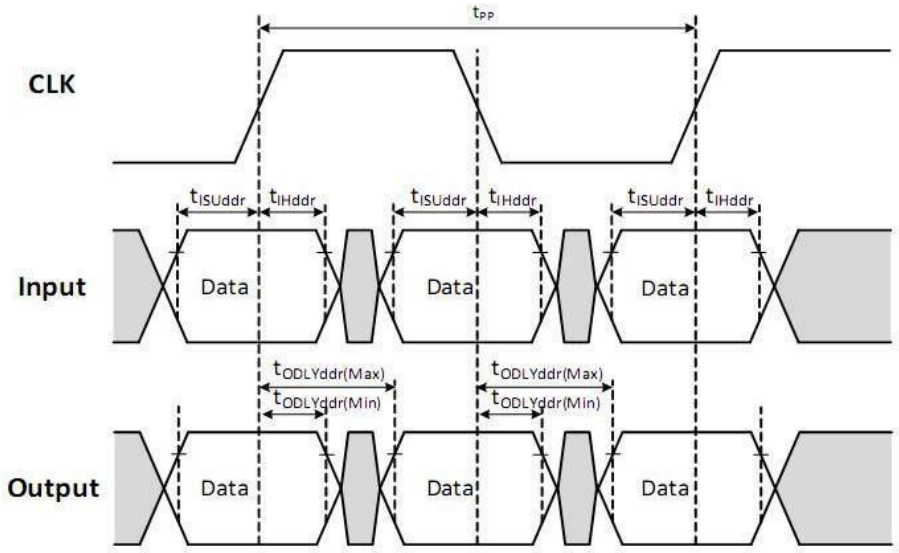
Parameter	Symbol	Min	Max	Unit	Remark
Open-drain bus signal level					
Output HIGH voltage	V_{OH}	VCCIO-0.2	-	V	-
Output LOW voltage	V_{OL}	-	0.3		I_{OL} = 2mA
Push-Pull signal level(2.7V~3.6V)					

Output HIGH voltage	V_{OH}	0.75*VCCIO	-	V	I_{OH} = -100μA @V_{ccQ} min
Output LOW voltage	V_{OL}				I_{OL} = 100μA @V_{ccQ} min
Input HIGH voltage	V_{IH}	0.625*VCCIO	VCCIO + 0.3		-
Input LOW voltage	V_{IL}	GNDIO – 0.3	0.25*VCCIO		-
Push-Pull signal level (1.70V~1.95V)					
Output HIGH voltage	V_{OH}	VCCIO – 0.45	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45*VCCIO		I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*VCCIO	VCCIO + 0.3		-
Input LOW voltage	V_{IL}	GNDIO – 0.3	0.35*VCCIO		-

6.3 Bus Timing

6.3.1. Bus Timing in SDR(Single Data Rate) Mode

Figure 5 Bus Timing in SDR Mode



6.3.2. Bus Timing in HS200 Mode

- HS200 Clock Timing

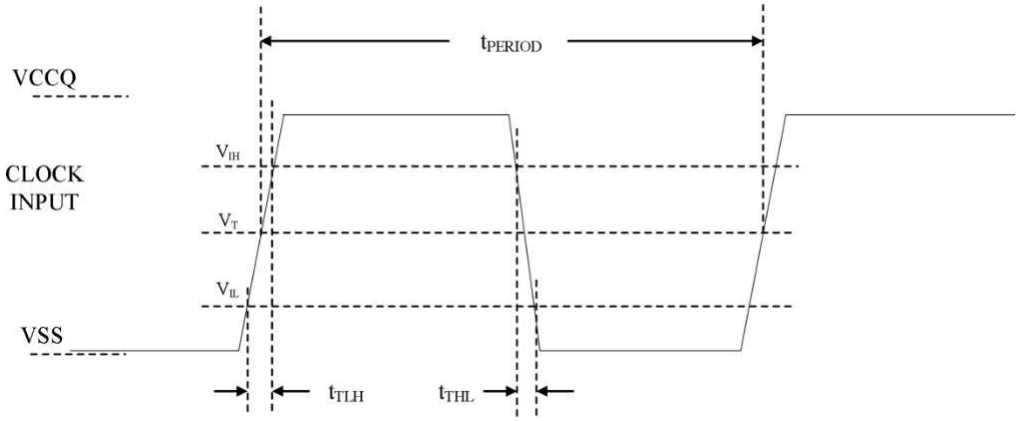
Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 6 and Table 7.

CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to

the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

Figure 6 HS200 Clock Signal Timing



Attention:

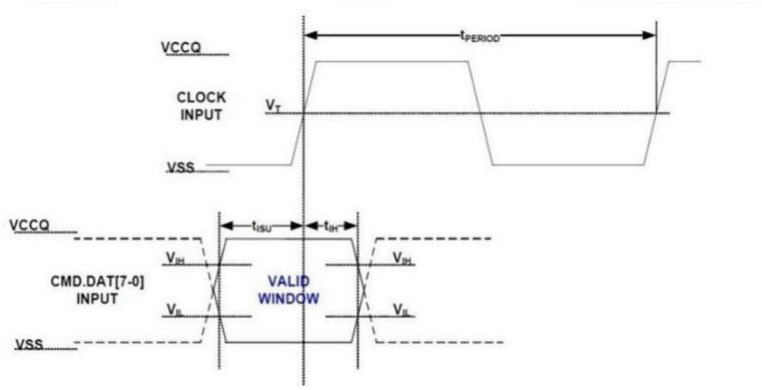
1. V_{IH} denotes VIH(Min.) and V_{IL} denotes V_{IL}(Max.).
2. V_T = 0.975V - Clock Threshold (VCCQ = 1.8V), indicates clock reference point for timing measurements.

Table 7 HS200 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2·t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (Max.) at 200MHz, CDEVICE = 6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty cycle	30	70	%	-

- HS200 Device Input Timing

Figure 7 HS200 Device Input Timing



Attention:

1. t_{ISU} and t_{IH} are measured at V_{IL}(max) and V_{IH}(min).
2. V_{IH} denotes V_{IH}(min) and V_{IL} denotes V_{IL}(max).

Table 8 HS200 Device Input Timing

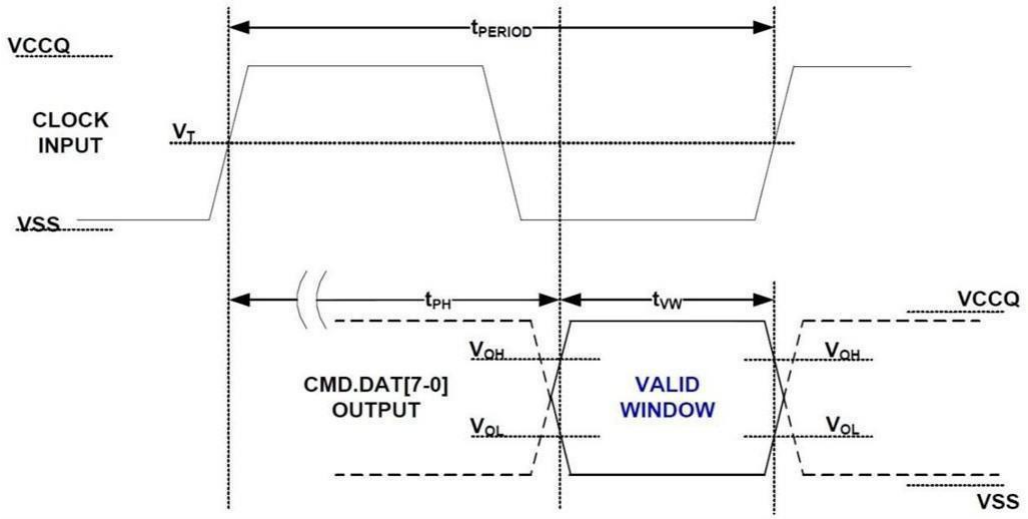
Symbol	Min	Max	Unit	Remark
t_{ISU}	1.40	-	ns	CDEVICE <= 6pF
t_{IH}	0.8	-	ns	CDEVICE <= 6pF

- HS200 Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD}. After initialization, the t_{PH} may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode. Figure 8, Table 9 define device output timing.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by Δt_{PH}. Output valid data window (t_{VW}) is available regardless of the drift (Δt_{PH}) but position of data window varies by the drift, as described in Figure 15.

Figure 8 HS200 Device Output Timing



Attention:

1. V_{OH} denotes V_{OH} (Min.) and V_{OL} denotes V_{OL} (Max.).

Table 9 HS200 Device Output Timing

Symbol	Min	Max	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long-term temperature drift.
Δt_{PH}	-350 (ΔT = -20℃)	+1550 (ΔT = 90℃)	ps	Delay variation due to temperature change aftertuning Total allowable shift of output valid window (t_{VW}) from last system Tuning procedure; refer to Figure & Table 15 for details. Δt_{PH} is 2600ps for ΔT from -25℃ to 125℃ during operation.

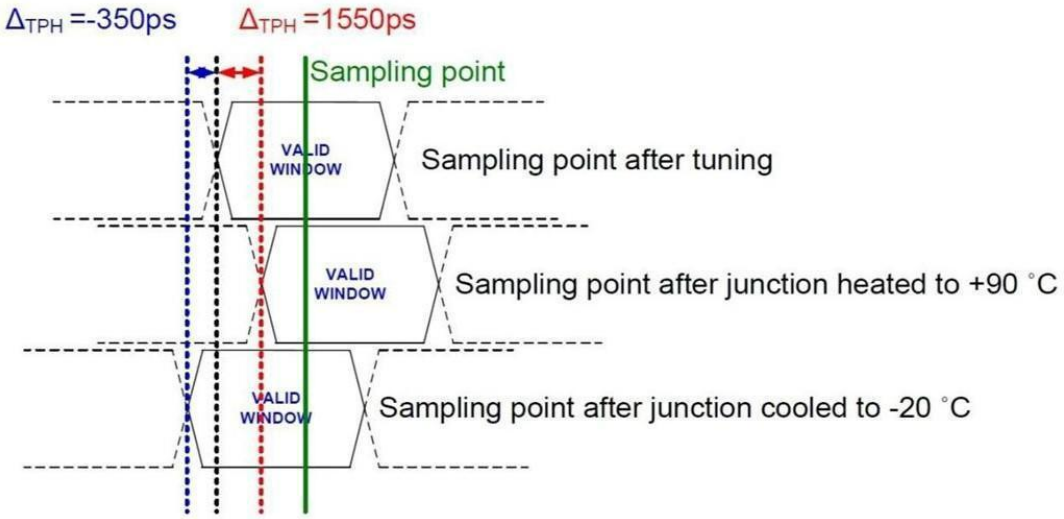
tvw	0.575	-	UI	tvw = 2.88ns at 200MHz Using test circuit in Figure 8, Table9, which includes skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected tvw at Host input is larger than 0.475UI.

Attention:

1. Unit Interval(UI) is one bit nominal time. For example, UI = 5ns at 200MHz.

- tPH Consideration

Figure 9 tPH Consideration



6.3.3. Bus Timing HS400 Mode

- HS 400 Device Input Timing

Figure 10 HS 400 Device Input Timing

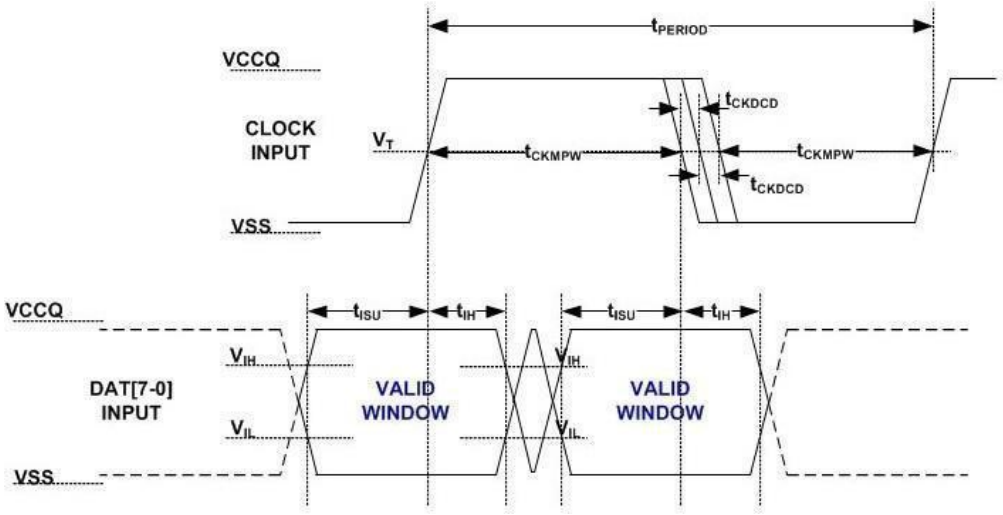


Table 10 HS 400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5	-	-	200MHz (Max.), between rising edges With respect to V_T
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle With respect to V_T Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2	-	ns	With respect to V_T
Input DAT (Referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4	-	ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH}/V_{IL}

- HS 400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

Figure 11 HS 400 Device Output Timing

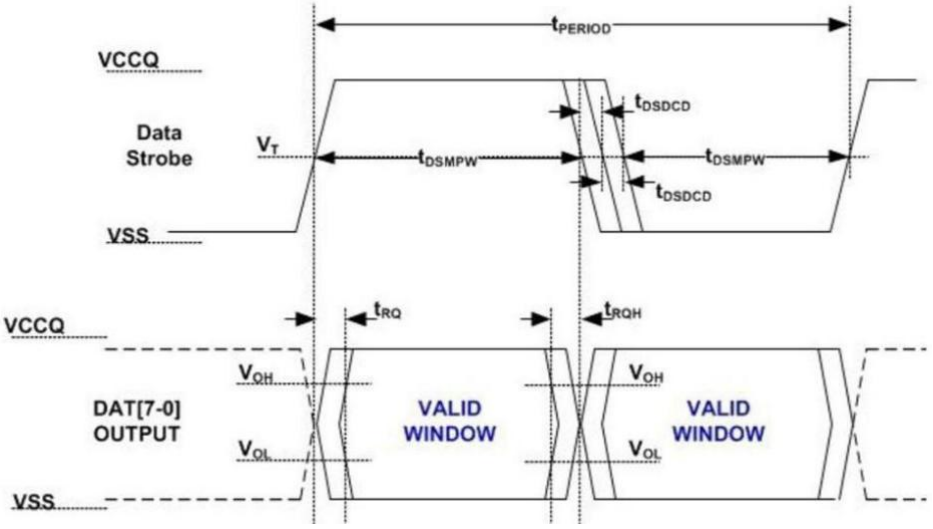


Table 11 HS 400 Device Output Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5		ns	200MHz(max), between rising edges. With respect to VT

SR	1.125		V/ns	Slew rate for Data Strobe and Output Data. With respect to VOH/VOL. HS400 reference load
t_{DSDCD}	0	0.2	ns	Data Strobe Duty cycle distortion. Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to VT Includes jitter, phase noise
t_{DSMPW}	2.0		ns	Data Strobe minimum pulse width With respect to VT
t_{RPRE}	0.4		t_{PERIOD}	Data Strobe Read pre-amble Max value up to infinite is valid
t_{RPST}	0.4		t_{PERIOD}	Data Strobe Read post-amble Max value up to infinite is valid
t_{RQ}		0.4	ns	With respect to VOH/VOL HS400 reference load
t_{RQH}		0.4	ns	With respect to VOH/VOL HS400 reference load

- HS400 Capacitance

Table 12 HS400 Capacitance

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Remark**
Pull-up resistance for CMD	RCMD	4.7	-	100	kΩ	-
Pull-up resistance for DAT[7:0]	RDAT	10	-	100		-
Pull-down resistance for data strobe	RDS	10	-	100		-
Internal pull-up resistance DAT[7:1]	Rint	10	-	150		-
Single device capacitance	CDevice	-	-	6	pF	-

7. eMMC Register

7.1 OCR Register

Table 13 OCR Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
Access Mode	[30:29]	Access Mode	0x02	2
VDD Range	[23:15]	VDD：2.7~3.6	0x1FF	9
	[14:8]	VDD：2.0~2.6	0x00	7
	[7]	VDD：1.70~1.95	0x01	1

7.2 CID Register

Table 14 CID Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
MMC MID	[127:120]	Manufacturer ID	0x37	8
Reserved	[119:114]	Reserved	---	6
Card/BGA	[113:112]	CBX	0x01	2
OEM/Application ID	[111:104]	OID	0x00	8
Product name	[103:56]	PNM	eMMC	48
Product revision	[55:48]	PRV	0x10/0x11[1]	8
Product Serial number	[47:16]	PSN	---	32
Manufacturing date	[15:8]	MDT	---	8
CRC7 checksum	[7:1]	CRC	---	7
Not used, always ‘1’	[0:0]	-	0x01	1

[1] *0x11 for Intel platform, 0x10 for standard platform but Intel*

7.3 CSD Register

Table 15 CSD Register

Parameter	DSR Slice Bit	Description	Value	Bit Width
CSD structure	[127:126]	CSD_STRUCTURE	0x03	2
System specification version	[125:122]	SPEC_VERS	0x04	4
Reserved	[121:120]	-	-	2
Data read access-time 1	[119:112]	TAAC	0x27	8
Data read access-time 2 in CLK cycles (NSAC*100)	[111:104]	NSAC	0x01	8
Max. bus clock frequency	[103:96]	TRAN_SPEED	0x32	8
Device command classes	[95:84]	CCC	0xF5	12
Max. read data block length	[83:80]	READ_BL_LEN	0x09	4
Partial blocks for read allowed	[79:79]	READ_BL_PARTIAL	0x00	1
Write block misalignment	[78:78]	WRITE_BLK_MISALIGN	0x00	1
Read block misalignment	[77:77]	READ_BLK_MISALIGN	0x00	1
DSR implemented	[76:76]	DSR_IMP	0x00	1
Reserved	[75:74]	-	-	2
Device size	[73:62]	C_SIZE	0xFFF	12
Max. read current @ VDD min	[61:59]	VDD_R_CURR_MIN	0x07	3
Max. read current @ VDD max	[58:56]	VDD_R_CURR_MAX	0x07	3
Max. write current @ VDD min	[55:53]	VDD_W_CURR_MIN	0x07	3
Max. write current @ VDD max	[52:50]	VDD_W_CURR_MAX	0x07	3
Device size multiplier	[49:47]	C_SIZE_MULT	0x07	3
Erase group size	[46:42]	ERASE_GRP_SIZE	0x1F	5
Erase group size multiplier	[41:37]	ERASE_GRP_MULT	0x1F	5
Write protect group size	[36:32]	WP_GRP_SIZE	0x1F	5
Write protect group enable	[31:31]	WP_GRP_ENABLE	0x01	1
Manufacturer default ECC	[30:29]	DEFAULT_ECC	0x00	2
Write speed factor	[28:26]	R2W_FACTOR	0x02	3
Max. write data block length	[25:22]	WRITE_BL_LEN	0x09	4
Partial blocks for write allowed	[21:21]	WRITE_BL_PARTIAL	0x00	1
Reserved	[20:17]	-	-	4
Content protection application	[16:16]	CONTENT_PROT_APP	0x00	1
File format group	[15:15]	FILE_FORMAT_GRP	0x00	1
Copy flag (OTP)	[14:14]	COPY	0x01	1
Permanent write protection	[13:13]	PERM_WRITE_PROTECT	0x00	1

Temporary write protection	[12:12]	TMP_WRITE_PROTECT	0x00	1
File format	[11:10]	FILE_FORMAT	0x00	2
ECC code	[9:8]	ECC	0x00	2
CRC	[7:1]	CRC	0x59	7
Not used, always'1'	[0:0]	-	0x01	1

7.4 Extended CSD Register

Table 16 Extended CSD Register

Parameter	DSR Slice Bit	Description	Value
EXT_SECURITY_ERR	[505]	Extended Security Commands Error	0x00
S_CMD_SET	[504]	Supported Command Sets	0x01
HPI_FEATURES	[503]	HPI Features	0x01
BKOPS_SUPPORT	[502]	Background operations support	0x01
MAX_PACKED_READS	[501]	Max packed read commands	0x20
MAX_PACKED_WRITES	[500]	Max packed write commands	0x20
DATA_TAG_SUPPORT	[499]	Data Tag Support	0x01
TAG_UNIT_SIZE	[498]	Tag Unit Size	0x00
TAG_RES_SIZE	[497]	Tag Resources Size	0x00
CONTEXT_CAPABILITIES	[496]	Context management capabilities	0x78
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0x01
EXT_SUPPORT	[494]	Extended partitions attribute support	0x03
SUPPORTED_MODES	[493]	FFU supported modes	0x01
FFU_FEATURES	[492]	FFU features	0x00
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	0x17
FFU_ARG	[490:487]	FFU Argument	0xFFFAFFF0
BARRIER_SUPPORT	[486]	Cache barrier support	0x01
CMDQ_SUPPORT	[308]	Command queue support	0x01
CMDQ_DEPTH	[307]	Command queue depth	0x1F
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAM MED	[305:302]	Number of FW sectors correctly programmed	0x00
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0x00
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B(TLC)	0x00
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A(SLC)	0x00
PRE_EOL_INFO	[267]	Pre EOL information	-
OPTIMAL_READ_SIZE	[266]	Optimal read size	0x40
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	0x40
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	0x07
DEVICE_VERSION	[263:262]	Device version	0x00
FIRMWARE_VERSION	[261:254]	Firmware version	FW Patch Ver.
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at	0x00